CLAIMS

The invention claimed is:

1. A semiconductor processing method for forming an electrical contact, comprising:

providing a semiconductor substrate having a surface suitable for electroless plating, a layer over the surface, and an electrically conductive node supported by the layer;

forming an opening through the layer and to the surface, a periphery of the opening including an electrically conductive portion of the electrically conductive node; and

electroless plating a conductive material within the opening and from the suitable surface, the electroless-plated material forming an electrical contact to the electrically conductive node.

2. The method of claim 1 wherein the layer is electrically insulative.

3. The method of claim 1 wherein an insulative material is over the node, and wherein the opening extends through the insulative material.

4. The method of claim 1 wherein the insulative material over the node is part of the layer supporting the node.

5. The method of claim 2 wherein the layer is comprised by a stack of two or more electrically insulative layers, and wherein the opening extends through the stack.

6. The method of claim 2 wherein the layer comprises BPSG.

7. The method of claim 1 wherein the opening is formed to a depth of at least about 3 microns.

8. The method of claim 1 wherein the electroless-plated conductive material comprises one or both of nickel and cobalt.

9. The method of claim 1 wherein the node includes an electrically conductive layer, and wherein the opening extends through the electrically conductive layer.

10. The method of claim 1 wherein the semiconductor substrate comprises a monocrystalline silicon base supporting a structure having the surface suitable for electroless plating.

11. The method of claim 10 wherein the structure is a block over the monocrystalline silicon base; and wherein the surface suitable for electroless plating is an uppermost surface of the block.

12. The method of claim 11 wherein the structure is a block over the monocrystalline silicon base; and wherein the surface suitable for electroless plating comprises one or more of palladium, zinc, silver, nickel and cobalt.

13. The method of claim 11 wherein the structure is a block over the monocrystalline silicon base; and wherein the surface suitable for electroless plating comprises one or both of nickel and cobalt.

14. A semiconductor processing method for forming an electrical contact, comprising:

providing a semiconductor substrate which supports an electrically insulative material and a pair of electrical nodes, the electrical nodes being a first node and a second node, a first opening extending through the electrically insulative material to the first node and a second opening extending through the electrically insulative material to the second node, the first node being at a first elevational height over the substrate and the second node being at a second elevational height over the substrate, the first elevational height being less than the second elevational height and accordingly the first opening being deeper than the second opening, the first electrical node having a first surface exposed within the first opening and the second electrical node having a second surface exposed within the second opening, the first surface being suitable for electroless plating and the second surface not being suitable for electroless plating;

electroless plating a first conductive material within the first opening and from the first surface to form a first conductive material plug extending to a height within the first opening that is about the same as the second elevational height;

activating the second surface to render the second surface suitable for electroless plating; and

after activating the second surface, electroless plating a second

conductive material within the first and second openings, the second conductive material within the first opening forming a second conductive material plug extending upwardly from the first conductive material plug, and the second material within the second opening forming a second conductive material plug extending upwardly from the second surface.

15. The method of claim 14 wherein the first and second conductive materials are compositionally the same as one another.

16. The method of claim 14 wherein the second conductive material plugs within the first and second openings extend to an upper surface of the electrically insulative material.

17. The method of claim 14 wherein the second conductive material plugs within the first and second openings extend upwardly beyond an upper surface of the electrically insulative material.

18. The method of claim 14 wherein the first node is part of a digit line and the second node is part of a capacitor electrode.

19. A semiconductor processing method for forming electrical contacts to a capacitor electrode and a digit line, comprising:

providing a semiconductor substrate, the semiconductor substrate supporting a digit line and a spacer structure, the digit line comprising a region and the spacer structure comprising another region; the digit line region having an upper surface and the spacer structure region having another upper surface, the digit line region upper surface being about the same elevational height over the substrate as the spacer structure region upper surface, the semiconductor substrate comprising a first insulative material over the digit line region and a second insulative material over the spacer structure region, the semiconductor substrate comprising a capacitor electrode supported by the substrate;

forming openings through the first and second insulative materials, the opening through the first insulative material being a first opening and extending to the upper surface of the digit line region, the opening through the second insulative material being a second opening and extending to the upper surface of the spacer structure region, the second opening having a periphery which includes an electrically conductive portion of the capacitor electrode; and

electroless plating a conductive material within the first and second openings, the electroless plating initiating from the upper surfaces of the digit line region and spacer structure region, the electroless-plated material forming an

electrical contact to the digit line in the first opening and forming an electrical contact to the capacitor electrode in the second opening.

20. The method of claim 19 wherein the capacitor electrode comprises one or more of TiN, WN, WSi and conductively-doped silicon, with the listed compositions being shown in terms of the elements contained therein rather than in terms of a particular stoichiometry of the elements within the compositions.

21. The method of claim 19 wherein the spacer structure is a dummy structure.

22. The method of claim 19 wherein the first and second insulative materials are comprised by a common layer.

23. The method of claim 22 wherein the common layer comprises BPSG.

24. The method of claim 22 wherein the common layer comprises a thickness of at least about 3 microns over the digit line region and spacer structure region.

25. The method of claim 22 wherein second opening extends through the capacitor electrode.

26. The method of claim 24 wherein the second opening extends through a segment of the capacitor electrode, and wherein the common layer comprises a thickness of less than or equal to about 1 micron over the segment of the capacitor electrode.

27. The method of claim 19 wherein the capacitor electrode is a capacitor plate electrode, the method further comprising:

forming a capacitor storage node electrode supported by the substrate;

forming at least one dielectric material over the capacitor storage node electrode; and

forming the capacitor plate electrode over the at least one dielectric material.

28. The method of claim 27 wherein the second opening extends through the capacitor plate electrode and the at least one dielectric material, but does not extend through the capacitor storage node electrode.

29. The method of claim 19 wherein the upper surfaces of the digit line region and spacer structure region have the same composition as one another prior to formation of the layer.

30. The method of claim 29 wherein the upper surfaces of the digit line region and spacer structure region have a suitable composition for the electroless plating prior to the formation of the layer.

31. The method of claim 30 wherein the suitable composition for the electroless plating comprises one or more of palladium, silver, zinc, nickel and cobalt.

32. The method of claim 30 wherein the suitable composition for the electroless plating comprises one or both of nickel and cobalt.

33. The method of claim 29 wherein the upper surfaces of the digit line region and spacer structure region do not have a suitable composition for the electroless plating prior to the formation of the layer, and are activated after the formation of the first and second openings to be suitable for the electroless plating.

34. The method of claim 33 wherein the activation comprises provision of a sufficient amount of one or more of palladium, silver, zinc, nickel and cobalt on the upper surfaces of the digit line region and spacer structure region to make the electroless plating spontaneous.

35. A semiconductor structure, comprising:

a semiconductor substrate;

a digit line supported by the semiconductor substrate, the digit line comprising a first region, the first region having an upper surface at a first elevational height over the semiconductor substrate;

a dummy structure supported by the semiconductor substrate, the dummy structure comprising a second region; and the second region having an upper surface at a second elevational height over the semiconductor substrate, the first and second elevational heights being about the same as one another;

a first insulative material supported by the semiconductor substrate and being over the digit line region;

a second insulative material supported by the semiconductor substrate and being over the dummy structure region;

a capacitor structure supported by the second insulative material, the capacitor structure including a first capacitor electrode, a second capacitor electrode and at least one dielectric material between the first and second capacitor electrodes;

a first conductive interconnect extending upwardly from the digit line region and through the first insulative material, the first conductive interconnect being of a composition; and

a second conductive interconnect extending upwardly from the

dummy structure region, through only one of the first and second capacitor electrodes and through the second insulative material; the second conductive interconnect being of the same composition as the first conductive interconnect.

36. The structure of claim 35 wherein said only one of the first and second capacitor electrodes comprises one or more of TiN, WN and WSi, with the listed compositions being shown in terms of the elements contained therein rather than in terms of a particular stoichiometry of the elements within the compositions.

37. The structure of claim 35 wherein the first and second insulative materials are comprised by a common layer.

38. The structure of claim 37 wherein the common layer comprises BPSG.

39. The structure of claim 37 wherein the common layer is over the capacitor structure and below the capacitor structure, and wherein the common layer comprises a thickness of at least about 3 microns proximate the digit line region and proximate the dummy structure region.

40. The structure of claim 39 wherein second conductive interconnect extends through a segment of said only one of the first and second capacitor electrodes, and wherein the common layer comprises a thickness of less than or equal to about 1 micron over said segment.

41. The structure of claim 35 wherein the second conductive interconnect extends through the at least one dielectric material.

42. The structure of claim 35 wherein the composition of the first and second conductive interconnects comprises one or more of palladium, silver, zinc, nickel and cobalt.

43. The structure of claim 42 wherein the composition of the first and second conductive interconnects comprises palladium.

44. The structure of claim 42 wherein the composition of the first and second conductive interconnects comprises silver.

45. The structure of claim 42 wherein the composition of the first and second conductive interconnects comprises zinc.

46. The structure of claim 42 wherein the composition of the first and second conductive interconnects comprises nickel.

47. The structure of claim 42 wherein the composition of the first and second conductive interconnects comprises cobalt.

48. A DRAM array comprising the structure of claim 42.

49. An electronic system comprising the DRAM array of claim 48.